



Creating the MK-III upgrade for the Sonic Frontiers SFD-2 (MK-I & MK-II)

A description of the upgrade design process, sonic challenges and jitter reduction in a two channel 24bit/96k High-End audio D/A converter.

Peter Schut

Sonic Frontiers International

Abstract

What to do when a highly regarded device, that got acclaimed recognition throughout the world needs an update that makes the unit ready for future sources with higher resolution. New sets of parameters arise when this happens. Jitter becomes more important, or at least the lack of jitter! Although jitter is widely accepted as a common artifact in today's digital audio systems, the effect of real-world jitter contamination is often underestimated. Several unique design considerations were made to improve the already wonderful sounding original. A discrete improved circuit replaces the Ultra Analog AES21 low jitter input receiver and the addition of an I2S.e input makes jitter contamination a thing of the past. The delicate D/A conversion is now performed by eight (8) Burr-Brown PCM1704 chips.

Input Circuit.

The input circuit uses 5 improved low capacitance high-speed relays. The circuit is changed in a way that unused inputs are now totally shut off. The new I2S.e input is placed on a daughter board above the main board. High speed low jitter ECL to TTL converters translate the balanced clocks coming out of an I2S.e based transport. The inputs are transformer coupled to reduce the chance of noise entering the chassis. This input was pioneered in the famous Processor 3. To have a similar performance with serial sources like AES/EBU or SPDIF on RCA, BNC, Toslink and ST, we investigated the behaviour of our new input circuitry with a special Jitter analyzer. (see side-bar "why jitter matters") We ended up with a dual PLL circuit.

Dual PLL topology

The capability of reliable data recovery and jitter attenuation needs a dual approach. If a circuit is capable of doing one discipline correctly, it is not capable of performing the other task with high precision. Therefore, the Sonic Frontiers design team decided to use a dual PLL topology. The input stage is based on the CS8414 together with several high bandwidth pulse transformers to incorporate a precise and reliable data recovery system. The second stage is a discrete PLL with

Why jitter matters

Clock Jitter

The jitter responsible for the loss of resolution and distortion in the analog reconstructed signal is clock jitter. This clock jitter is either the wordclock or masterclock of the D/A converter chip. Depending on the conversion principle used by the actual converter, either the masterclock or wordclock needs to be jitter free. The jitter measured at this point is the timing deviation of the transitions compared to an ideal clock. These timing variations are divided into a jitter frequency and amplitude. Examining the eye pattern of these clocks with an oscilloscope can tell you something of the peak to peak value, but gives you no information of the jitter frequency. Using an oscilloscope for jitter amplitudes lower than 1ns is almost impossible. So we need a dedicated jitter analyzer.

custom made VCXOs. Two VCXOs are used per channel to decode the four most popular clock frequencies of 44.1 kHz and 88.2 kHz with the first VCXO and 48 kHz and 96 kHz with the second VCXO. A new highly improved phase comparator is used to perform a lock mechanism without the common “dead zone” found in most other phase comparators and PLL circuits. This also lowered the intrinsic jitter.

Intrinsic Jitter and Jitter attenuation

An essential characteristic of a high performance audio D/A converter is the intrinsic jitter of the device when a “jitter free” source is connected. The CS 8414 has an intrinsic jitter of approximately 150 to 200 ps RMS. To fully use the resolution of the 24 bit D/A converter chips in the SFD2-MKIII, the second PLL has an intrinsic jitter of 2 ps RMS. Together with a jitter attenuation frequency of 10 Hz and a jitter attenuation capability of over 60 dB, the robust input can handle input signals with extreme jitter contamination without degradation of the total performance.

Signal degradation without a dual PLL approach.

If we look at a test signal based on a normal AES/EBU data stream, but with the insertion of a normal 300-foot AES/EBU cable, (This is a standard test in the “Audio Precision System 2 Cascade” and could well simulate a bad transport) the performance degradation of single PLL topologies becomes obvious.

Figure 1 displays the eye pattern of an AES/EBU signal when it travels direct or through a 300-foot cable simulator.

Figure 2 shows the intrinsic jitter of both the first and the second PLL of the SFD2-MKIII when fed direct from the “Audio Precision System 2 Cascade”

Figure 3 displays the use of the 300-foot cable simulator and the degradation of the clock jitter performance induced by the frequency limitation of the cable’s low-pass function. The increase in jitter is obvious and also the jitter attenuation characteristic of the second PLL. This second PLL starts attenuating the jitter at 10 Hz and rapidly lowers the jitter to insignificant values. The single bin residual jitter values are as low as 50 femto seconds (= 0.05 ps).

The dual PLL also provides us a measured frequency indication. This indication is routed to the front panel. As the original SFD2-MKI and MKII were not capable of decoding above 48kHz sampling and the front panel was therefore not equipped with these indicators we decided to abandon 32kHz sampling and use this LED as 2x indicator. So when a digital source is selected that has a 96kHz sampling frequency the LED’s for 48k and FS x 2 will be on. For 88.2kHz both the LED’s 44.1 and FS x 2 will lit!

The PMD-200 Digital over-sample filter and HDCD® decoder

The main reason to upgrade the wonderful SFD2-MKII was the introduction of the PMD-200. When we improved the MKI to MKII the most important sonic advantages were due to the PMD-100. This HDCD®

The Jitter Analyzer Sonic Frontiers is using has an intrinsic jitter of 0.4 ps RMS for a clock frequency of 12.288 MHz (=256 x 48 kHz) and 1.2 ps for 192 kHz (=4 x 48 kHz).

High frequency jitter causes more audible degradation than low frequency jitter. High frequency signals are also more degraded by a certain amount of jitter than low frequency signals.

Interface Jitter

Interface jitter is probably the biggest contributor to the overall jitter performance of a system. In particular, the bandwidth limitations of twisted pair digital audio connections can cause severe degradation of the overall performance in a D/A converter. Because of the inherent bandwidth limitation of the interface cable, the waveform change of the AES/EBU signal causes severe degradation of the timing resolution in commonly used receiver chips. The industry standard Crystal semiconductor CS8412 and CS8414 (for 96k) has a jitter attenuation frequency of 25kHz. This is the frequency at which the integral PLL starts to attenuate the incoming jitter. Baring in mind that the jitter frequency of any concern ranges up to 40kHz, we can conclude that the jitter attenuation capabilities of these chips are insignificant. The big advantage of these chips is the capability to reliably lock to difficult jittery signals of various amplitudes with good integrity. This is key to robust functioning of a D/A converter.

decoder and 8 times over-sampling filter was a huge step forward. Not only with HDCD® encoded disks but also with no encoded disks this filter proved to be a sonic winner. Although the 96kHz capability was available before the PMD-200 we didn't want to leave this sonic character and use a different filter. The PMD-200 is a DSP based chip. The core is a Motorola DSP where the HDCD code is already added. The use of a DSP in a design brings new challenges and a small micro-controller was also needed. This controller initializes the DSP every time an input condition changes. Three jumpers are used for user adjustable presets. One jumper is used to engage the digital domain 6dB attenuation that is part of the HDCD® specification. In normal use we advise to discard the digital attenuation and use the pre-amp to compensate for average loudness levels. The 2 other jumpers will be used for future firmware upgrades (adding dither is one of the settings we are investigating, and one of the features of the PMD-200)

Power supply and 4 layer PCB

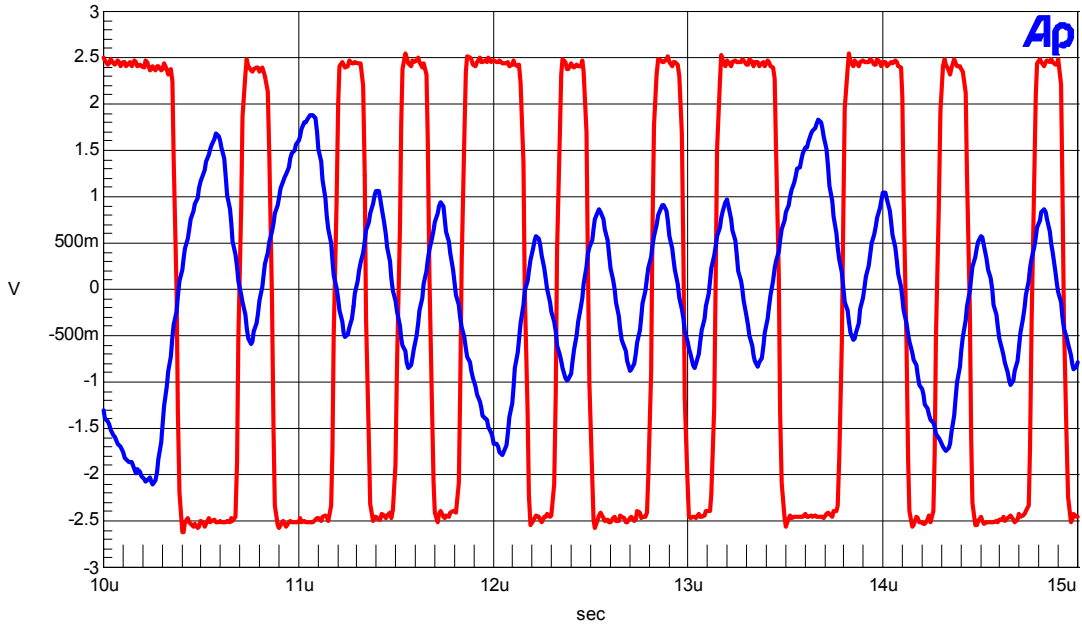
Dedicated power supplies and a 4 layer PCB are responsible for a low noise and low jitter environment. The use of 4 layer PCBs is quite unique in High-End audio. The advantages are numerous as we can pour a solid plane for the ground and maintain optimum current return paths for digital circuits. In the analog domain the advantages are different. Here we create a solid plane for the positive and negative supply rails and create a very high-speed power source for the delicate analog functions. Because the power supply is everywhere a circuit just needs to “grab down” and is connected to the supply of fast and noise-free energy. Cascaded regulators (both types based on high performance LT types) are used to supply the plus and minus five volt for the D/A converter chips. The D/A converters are placed on the analog part of the upgrade PCB and data is applied to these regions with series resistors to cancel out noise coupling.

D/A converters and I/V conversion

The actual D/A conversion is performed by eight (8) Burr-Brown PCM1704 converter chips. These chips are placed in a fully balanced topology with 2 converters in parallel per channel per phase. This topology reduces noise and distortion, and increases linearity. The digital audio is converted to a fully balanced signal right after the PMD-200 and stays balanced all the way to the output connectors. The PCM1704 is one of the best D/A converters in the market today. Its performance however is fully depending on the quality of the current to voltage conversion after the chip. Because the PCM1704 is a current output D/A converter chip, a I/V stage needs to be added to convert the waveform that is present in Current to a Voltage that can be used to listen to. A simple but very linear concept is using a simple resistor to ground. Although this approach give a near perfect linearity its output voltage is low when a low noise figure needs to be maintained. We chose for an active approach where an ideal amp with perfect resistor is used. The amp is the Burr-Brown OPA627, an operational amplifier with high speed, low noise. “no” distortion and ideal extreme high input impedance. This amplifier does not only perform excellent on paper and in measurements, it also sounded the best of all operational amplifiers we tested. The resistor is a “Vishay” bulk metal film type with low inductance and noise. Warmth, transparency, speed and smoothness where key words described by members of the listening panel.

MK-III

All the above-mentioned design considerations make the MK-III a trustworthy successor to the MK-II. Not only did we improve the technical performance like 96k capability and I2S.e input. We also lowered (and almost removed) the sensitivity to transport and interface jitter. The parallel converter chips, first rate I/V stage and 4 layer PCB with extensive power-supply regulation shifted the MK-III to a higher sonic level.



ms

Figure 1:
AES/EBU signal before and after 300-foot twisted-pair

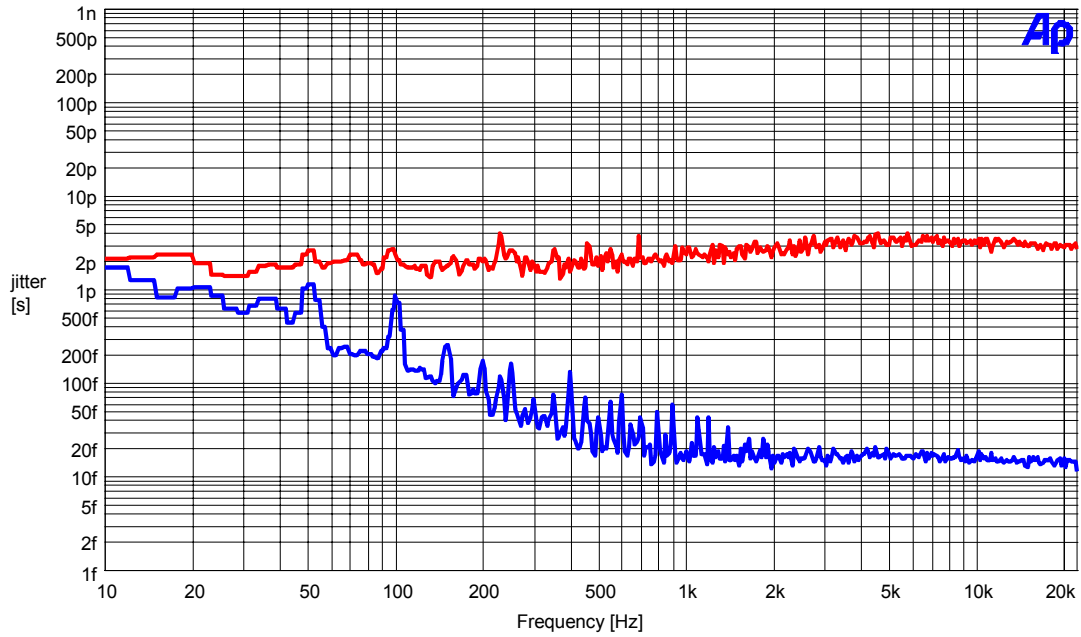


Figure 2:
Intrinsic jitter of SFD2-MKIII top trace (red) first PLL bottom trace (blue) second PLL
The RMS values calculate to 150 ps and 2 ps respectively

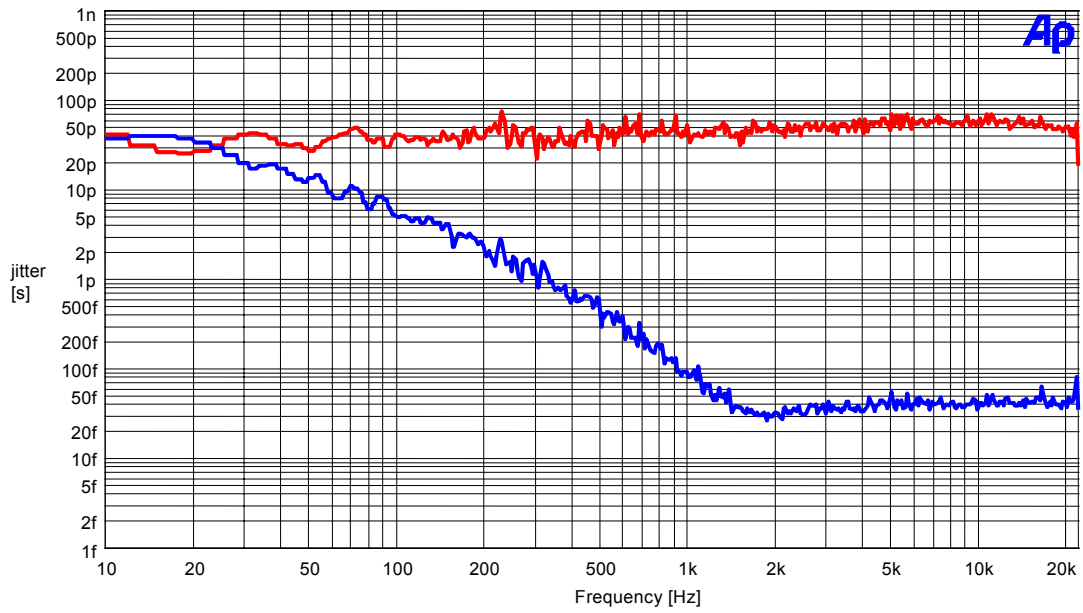


Figure 3:
jitter of SFD2-MKIII top trace (red) first PLL bottom trace (blue) second PLL with use of a 300-foot cable simulator. The RMS values calculate to 2.7 ns and 35 ps respectively
